## Controller – APE

### General Overview

This module, which is abbreviated to dla\_crtl\_ape, is used to generate control signals to control APE according to the different work modes and provide correct address when APE needs to read or write data from global buffer.

### I/O Definition

**Table 1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signals** | **Direction** | **Bit Width** | **Description** |
| **Global Signals** | | | |
| clk | input | 1 |  |
| rst | input | 1 |  |
| **Instruction Signals** | | | |
| start\_comp\_ape | input | 1 | Start signal of the computation of APE |
| stgr\_ape\_gb\_addr\_sa | input | 1 | Start address of source a |
| stgr\_ape\_gb\_addr\_sb | input | 13 | Start address of source b |
| stgr\_ape\_gb\_addr\_d | input | 13 | Start address of the destination |
| stgr\_ape\_len | input | 13 | Data length that the APE need to handle,0-indexed |
| stgr\_ape\_mode | input | 3 | The type of the operation that the APE need to execute |
| stgr\_ape\_imm | input | 16 | The immediate number, used when APE works in immediate ADD mode or immediate MUL mode |
| **Ctrl Signals** | | | |
| ctrl\_ape\_sa\_en | output | 1 | Enable signal to read source a |
| ctrl\_ape\_ab\_en | output | 1 | Enable signal to access ab buffer |
| ctrl\_lpe\_sb\_en | output | 1 | Enable signal to read source b |
| ctrl\_ape\_mul\_en | output | 1 | Enable signal of the multiplier in APE |
| ctrl\_ape\_add\_en | output | 1 | Enable signal of the adder in APE |
| ctrl\_ape\_mode | output | 3 | The type of the operation that the APE need to execute, directly connected to stgr\_ape\_mode |
| ctrl\_ape\_imm | output | 16 | The immediate number, directly connected to stgr\_ape\_imm |
| bif\_gb\_ape\_addr | output | 13 | The address of global buffer that the APE need to access |
| bif\_gb\_ape\_wen | output | 1 | Write enable signal to access global buffer |
| bif\_gb\_ape\_ren | output | 1 | Read enable signal to access global buffer |
| complete\_comp\_ape | output | 1 | Complete signal of current operation of APE |

### Description

The APE can do five different types of operations. Every type has its unique pipeline in order to avoiding empty bubble. Because of the difference of pipelines, the time sequences of control signals in different pipelines are also different. The APE controller use a fsm to help generate corresponding control signals for different pipelines. The picture below is the diagram of the fsm.



Figure 1. Diagram of the FSM in APE

And the time sequence of control signals under different situations are shown below. We assume that the APE processing corresponding function twice continuously(the value of stgr\_ape\_len is 1, 0-indexed).

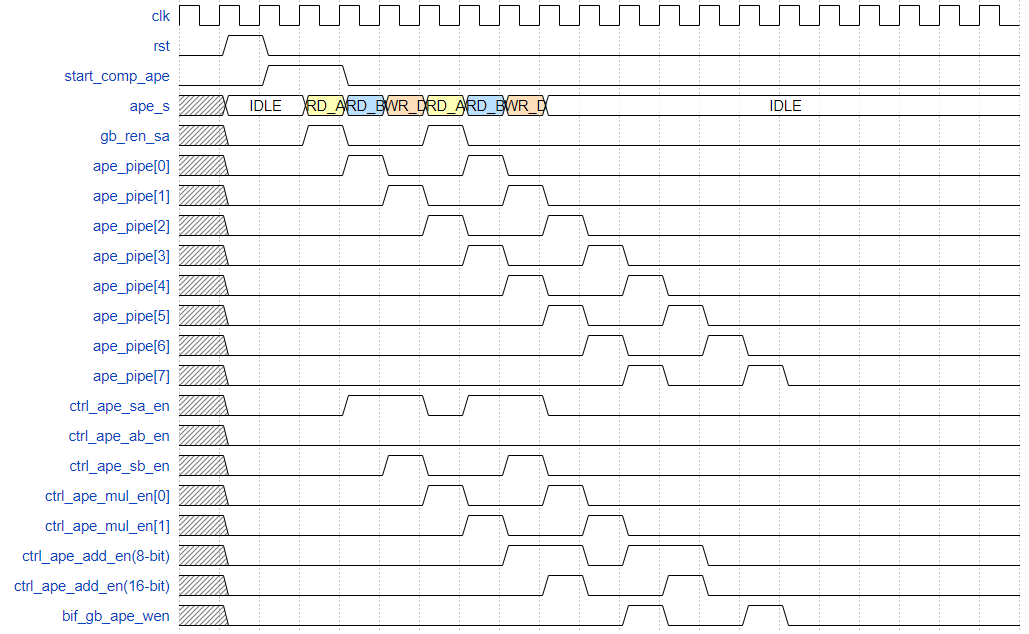


Figure 2. Elementwise Multiplication

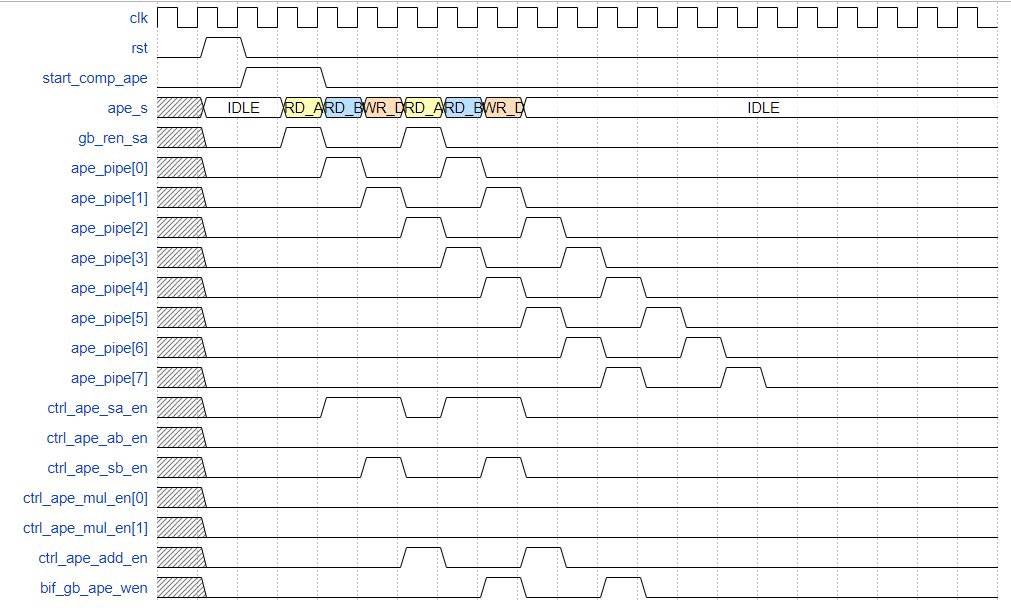


Figure 3. Elementwise Addition

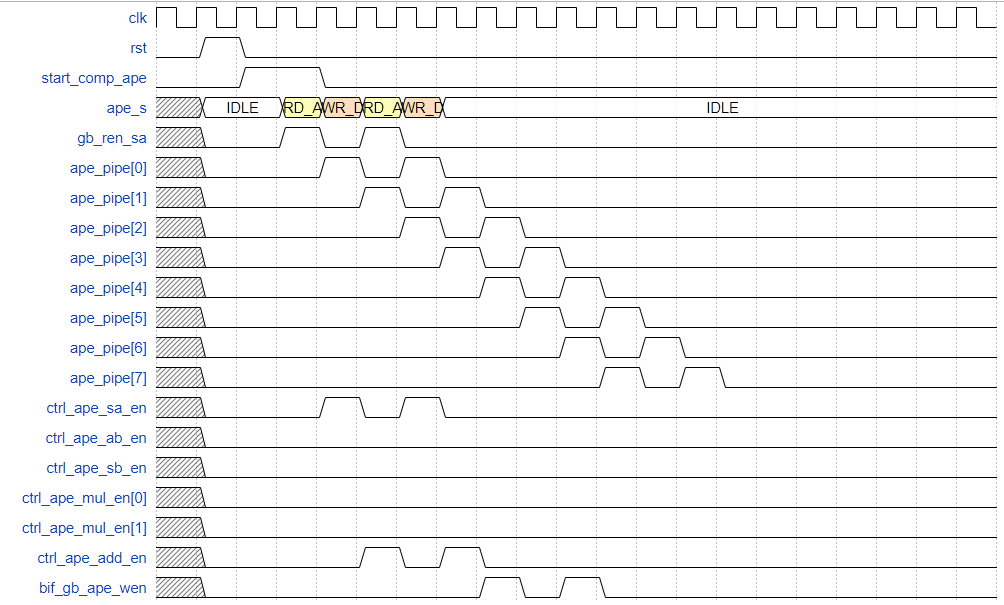


Figure 4. Addition with an Immediate Number

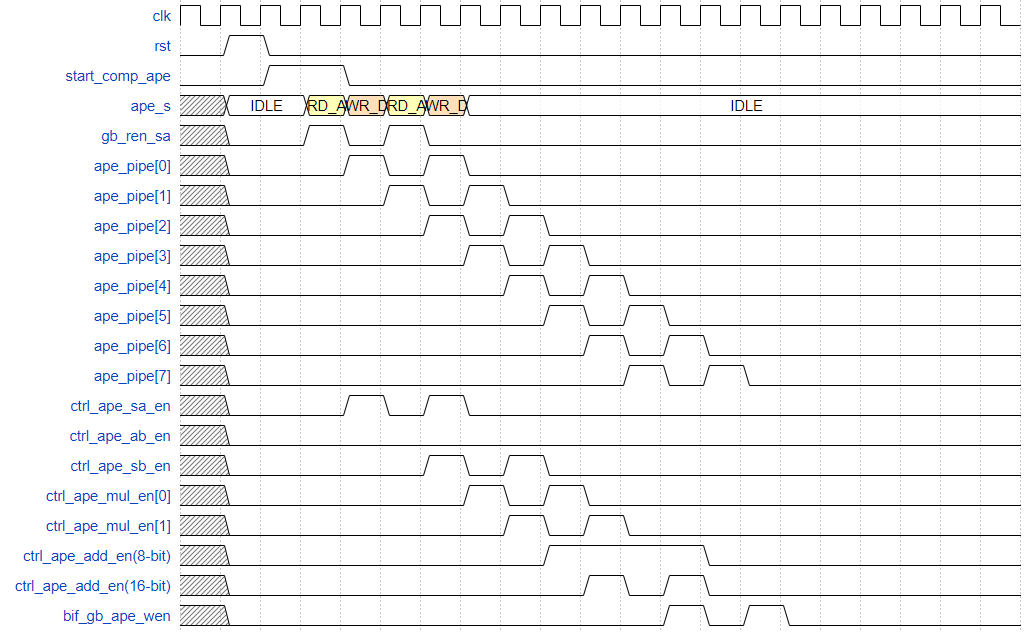


Figure 5. Multiplication with an Immediate Number

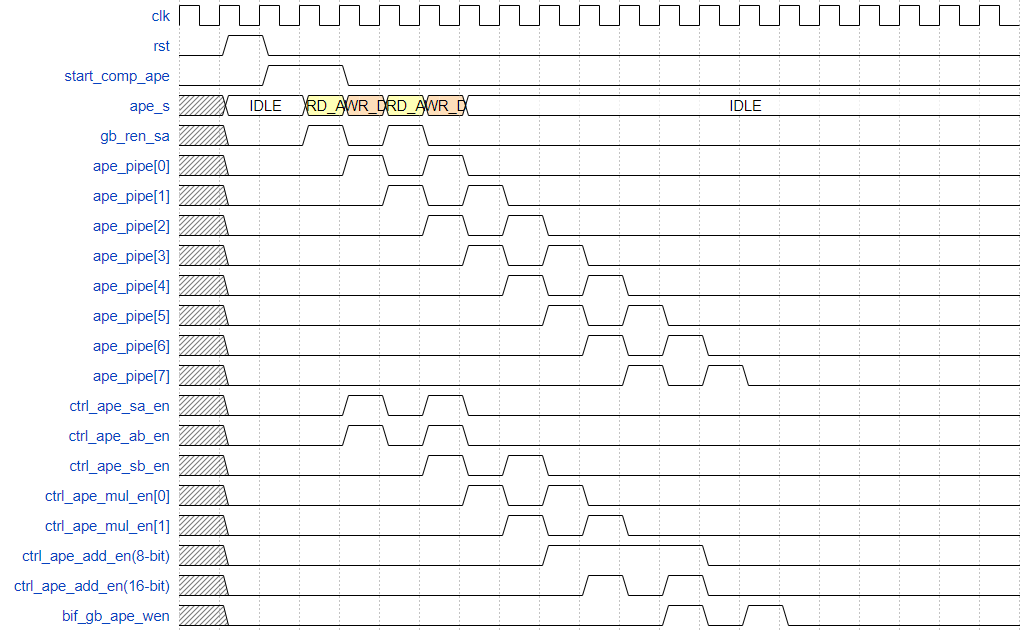


Figure 6. Activation Function

Besides generating control signals, this controller also calculates the address of global buffer that the APE needed to read(source) or write(destination) data. Because in some functions, the APE needs two source data and both two addresses are calculated in the same way. So the controller need to calculate two source addresses and one destination address. We can see the corresponding logic below.



Figure 7. Logic of source address generation

The pattern about the change of cnt\_len can be find in the diagram of control fsm.



Figure 8. Logic of destination address generation

The pattern about the change of bif\_gb\_ape\_wen can be find in the diagram of control fsm.

The final output address to APE is selected by corresponding enable signals(can find in the I/O defination).



Figure 9. Logic of complete\_comp\_ape

When the operation complete, the controller will output a complete signal. The picture above is the logic about complete signal(complete\_comp\_ape). The picture below shows the logic about cnt\_len\_d.



Figure 10. Logic about cnt\_len\_d